CLAIMS

What is claimed is:

1. A digital video processor comprising:

an error memory and a merge memory;

a half pixel filter communicably coupled to the merge memory;

a controller communicably coupled to the error memory, the merge memory and the half pixel filter, the controller executing one or more instructions to provide motion compensation during video decoding; and

a sum unit communicably coupled to the error memory and the merge memory.

2. The digital video processor as recited in claim 1, wherein the half pixel filter is programmable.

3. The digital video processor as recited in claim 1, wherein the error memory and the merge memory are random access memory.

4. The digital video processor as recited in claim 1, further comprising:

an error buffer communicably coupled to the error memory;

an instruction buffer communicably coupled to the controller;

a reference buffer communicably coupled to the half pixel filter; and

a display buffer communicably coupled to the sum unit.

5. The digital video processor as recited in claim 4, wherein the error buffer, the instruction buffer, the reference buffer and the display buffer are random access memory.

6. The digital video processor as recited in claim 1, wherein the one or more instructions includes at least one of a load instruction, a merge instruction and a write instruction.

7. The digital video processor as recited in claim 1, wherein the controller further comprises:

an instruction queue;

an execution unit communicably connected to the instruction queue and the error memory; and

a motion compensation state machine communicably connected to the execution unit, the half pixel filter and the merge memory.

8. The digital video processor as recited in claim 1, wherein the sum unit utilizes at least one or more error terms stored in the error memory with one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock.

9. The digital video processor as recited in claim 1, wherein the half pixel filter performs vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector.

10. A digital video processor comprising:

an error memory configured to store one or more error terms;

a merge memory configured to store one or more filtered prediction blocks;

a filter communicably coupled to the merge memory, the filter configured to perform vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector;

an instruction queue configured to store one or more instructions;

an execution unit communicably coupled to the instruction queue and the error memory, the execution unit configured to receive an instruction from the instruction queue, determine whether the error memory is full and send the instruction to a motion compensation state machine for execution;

the motion compensation state machine communicably coupled to the execution unit, the filter and the merge memory, the motion compensation state machine configured to execute the instruction received from the execution unit; and

a sum unit communicably coupled to the error memory and the merge memory, the sum unit utilizes at least one or more error terms stored in the error memory with one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock.

11. The digital video processor as recited in claim 10, wherein the filter and the motion compensation state machine are programmable.

12. The digital video processor as recited in claim 10, further comprising:

an error buffer communicably coupled to the error memory;

an instruction buffer communicably coupled to the controller;

a reference buffer communicably coupled to the half pixel filter; and

a display buffer communicably coupled to the sum unit.

13. The digital video processor as recited in claim 10, wherein the motion compensation state machine is further configured to execute a load instruction, a merge instruction or a write instruction.

14. A digital video processor comprising:

an error buffer;

an error memory communicably coupled to the error buffer, the error memory configured to receive and store one or more error terms from the error buffer;

an instruction buffer;

an instruction queue communicably coupled to the instruction buffer, the instruction queue configured to receive and store one or more instructions from the instruction buffer;

a merge memory configured to receive and store one or more filtered prediction blocks;

a reference buffer;

a half pixel filter communicably coupled to the reference buffer and the merge memory, the half pixel filter performing vertical and horizontal half-pixel interpolation on a prediction block received from the reference buffer as dictated by a motion vector to produce a filtered prediction block, and writing the filtered prediction block to the merge memory;

an execution unit communicably coupled to the instruction queue and the error memory, the execution unit configured to receive an instruction from the instruction queue, determine whether the error

memory is full and send the instruction to a motion compensation state machine for execution;

the motion compensation state machine communicably coupled to the execution unit, the half pixel filter and the merge memory, the motion compensation state machine configured to execute the instruction received from the execution unit; and

a sum unit communicably coupled to the error memory and the merge memory, the sum unit utilizing at least one or more error terms stored in the error memory and one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock, and to write the decoded macroblock to an display buffer.

15. The digital video processor as recited in claim 14, wherein the half pixel filter and the motion compensation state machine are programmable.

16. A method for providing video motion compensation comprising the steps of:

receiving one or more prediction blocks;

receiving one or more instructions;

receiving one or more error terms; and

utilizing at least the one or more prediction blocks and the one or more error terms as directed by the one or more instructions to produce a decoded macroblock.

17. A method for providing video motion compensation comprising the steps of:

receiving an instruction and writing the instruction to an instruction queue;

moving the instruction from the instruction queue to an execution unit if the execution unit is not full;

receiving an error term and writing the error term to an error memory;

executing the instruction in the execution unit if the instruction is not a write instruction; and

if the instruction in the execution unit is a write instruction, waiting until the error memory is full, and then utilizing at least all the error terms stored in the error memory and one or more prediction blocks stored in a merge memory to produce a decoded macroblock.

18. The method for providing video motion compensation as recited in claim 17, wherein the step of executing the instruction in the execution unit if the instruction is not a write instruction further comprises the step of if the instruction in the execution unit is a load instruction, reading a prediction block from a reference buffer, utilizing at least the prediction block and a half pixel filter to produce a filtered prediction block, and writing the filtered prediction block to a merge memory.

19. The method for providing video motion compensation as recited in claim 17, wherein the step of executing the instruction in the execution unit if the instruction is not a write instruction further comprises the step of if the instruction in the execution unit is a merge instruction, reading a prediction block from a reference buffer, utilizing at least the prediction block and a half pixel filter to produce a filtered prediction block, and merging the filtered prediction block with one or more previously filtered prediction blocks.

20. A system for providing video motion compensation comprising:

a video decoder configured to produce one or more instructions and one or more error terms;

a picture memory; and

a digital video processor comprising an error memory communicably coupled to the video decoder, a half pixel filter communicably coupled to the picture memory, a merge memory communicably coupled to the half pixel filter, a controller communicably coupled to the video decoder, the error memory, the merge memory and the half pixel filter, a sum unit communicably coupled to the error memory, the merge memory and the picture memory, and the controller executing the one or more instructions to provide motion compensation.

21. The system for providing video motion compensation as recited in claim 20, further comprising:

an error buffer communicably coupled between the error memory and the video decoder;

an instruction buffer communicably coupled between the controller and the video decoder;

a reference buffer communicably coupled between the half pixel filter and the picture memory; and

a display buffer communicably coupled between the sum unit and the picture memory.

22. The system for providing video motion compensation as recited in claim 21, wherein the error memory, the merge memory, the picture memory, the error buffer, the instruction buffer, the display buffer and the reference buffer are static random access memory.